(Please write your Exam Roll No.) Exam Roll No. .....

END TERM EXAMINATION

FIFTH SEMESTER [B.TECH.]- DECEMBER 2009

Paper Code: ETCS-305 **Subject: Computer Architecture**
Paper ID: 27305

Time : 3 Hours **Maximum Marks :75**

Note: Attempt any five questions in all. Q.No.1 is compulsory. Attempt one question from each unit.

Q.1	(a)	Explain register transfer language.	(5)
	(b)	Explain stack organization.	(5)
	(c)	Explain priority interrupt.	(5)
	(d)	Discuss memory hierarchy.	(5)
	(e)	Discuss characteristics of multiprocessor.	(5)

UNIT-I

Q.2	(a)	Explain timing sequence of instruction cycle.	(6.5)
	(b)	Explain architecture of Computer System.	(6)
		OR	
Q.3	(a)	Design a Accumutator logic for computers system.	(6.5)
	(b)	Differentiae between direct and indirect addressing. Discuss various technique for the same.	(6)

UNIT-II

Q.4	(a)	Differentiate between RISC and CISC.	(6.5)
	(b)	Explain instruction format of computer system.	(6)
		OR	
Q.5	(a)	Explain pipeline processing of instruction.	(6.5)
	(b)	Explain array processor.	(6)

UNIT-III

Q.6	(a)	Explain Booth Algorithm in detail.	(6)
	(b)	Explain MAR.	(3)
	(c)	Explain floating point number representation.	(3.5)
		OR	
Q.7	(a)	Explain Isolater and Memory mapped I/O.	(4)
	(b)	Define strobe control.	(4)
	(c)	Explain UART.	(4.5)

UNIT-IV

Q.8	(a)	Explain the organization of virtual memory.	(6)
	(b)	Assume system has 48-bit virtual address, 36 bit physical address, 128 MB of main memory and page size in the system is 4096 byte (4KB) pages. Find systems support to how many virtual and physical pages in the address space.	(6.5)
		OR	
Q.9	(a)	Explain CAM.	(6)
	(b)	Explain interconnection structure of computer system.	(6.5)

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